IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A circuit, comprising:

a n-channel differential amplifier having a first input transistor and a second input transistor that delivers current to a summing node, wherein the first and the second input transistors receive bias currents, and wherein the n-channel differential amplifier has a common mode output voltage; and

a first n-channel common source amplifier and a second n-channel common source amplifier coupled to the n-channel differential amplifier, wherein the first and the second common source amplifiers have a first output and a second output to provide a negative common mode feedback that is coupled to the summing mode;

a feedback circuit coupled to the first and the second outputs of the n-channel common source amplifier circuits, wherein the feedback circuit provides more current to the summing node if voltages at the first and the second outputs rise above a common mode reference voltage; and

a biasing circuit coupled to the feedback circuit and the n-channel differential amplifier, wherein the biasing circuit provides a constant current to the summing node, wherein the bias currents through the first and the second input transistors are reduced if a common mode voltage at the first and the second outputs rise above a common mode reference voltage.

2. (Canceled)

3. (Currently Amended) The circuit of claim [[2]] 1, further comprising:

a level shifter circuit coupled to the differential amplifier to adjust the first common mode output voltage.

4-6 (Canceled)

7. (Currently Amended) The circuit of claim [[6]] 1, wherein the common mode output voltage of the n-channel differential amplifier increases if the bias currents through the first and the second input transistors are reduced.

8. (Original) The circuit of claim 7, wherein the common mode output voltage of the first and the second common source amplifiers is reduced if the common mode output voltage of the n-channel differential amplifier increases.

9. (Original) The circuit of claim 1, wherein the n-channel differential amplifier, the first n-channel common source amplifier, and the second n-channel common source amplifier comprise transistors having gate widths less than or equal to 0.25 micron.

10. (Currently Amended) An operational amplifier, comprising:

a first gain stage having an inverting common mode gain, wherein the first gain stage comprises a first input transistor coupled to a summing node and a second input transistor coupled to the summing node, wherein the first gain stage outputs a common mode voltage; and

a second gain stage coupled to the first gain stage, wherein the second gain stage provides a negative common mode feedback to the first gain stage, wherein the second gain

stage outputs a common mode voltage, wherein the second gain stage comprises a first output signal and a second output signal, wherein current supplied to the summing node through the first and the second transistors is decreased if the common mode output voltage of the second gain stage is increased, wherein the common mode output voltage of the first gain stage is increased if the current supplied to the summing node through the first and the second transistors is decreased.

11. (Original) The operational amplifier of claim 10, further comprising:

a biasing circuit coupled to the summing node, wherein the biasing circuit sinks a constant current from the summing node.

12. (Canceled)

13. (Currently Amended) The operational amplifier of claim [[12]] 10, wherein the common mode output voltage of the second stage is decreased if the common mode output voltage of the first stage is increased.

14-21 (Canceled)